

**IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
AUSTIN DIVISION**

FREESCALE SEMICONDUCTOR, INC.	§	CIVIL ACTION NO. 1:12-cv-644-LY
	§	(LEAD CASE)
Plaintiff,	§	
	§	
v.	§	
	§	
FUNAI CORPORATION, INC.;	§	
FUNAI ELECTRIC CO, LTD.;	§	
CSR TECHNOLOGY, INC.; ZORAN	§	
CORPORATION; MEDIATEK INC.;	§	
MEDIATEK USA INC.;	§	
VIZIO, INC.; SANYO ELECTRIC CO., LTD.;	§	
SANYO NORTH AMERICA CORPORATION;	§	
SANYO MANUFACTURING	§	
CORPORATION; TPV TECHNOLOGY	§	
LIMITED; TPV INTERNATIONAL (USA)	§	
INC.; TOP VICTORY ELECTRONICS	§	
(TAIWAN) CO., LTD.; TOP VICTORY	§	
ELECTRONICS (FUJIAN) CO., LTD.;	§	
ENVISION PERIPHERALS, INC.; AMTRAN	§	
TECHNOLOGY CO., LTD;	§	
AMTRAN LOGISTICS, INC., AND	§	
MARVELL SEMICONDUCTOR, INC.	§	
	§	
Defendants.	§	

JOINT CLAIM CONSTRUCTION STATEMENT

Pursuant to the Court's Scheduling Order issued on January 14, 2013, the parties hereby submit this Joint Claim Construction Statement.

Dated: July 8, 2013

Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document via the Court's CM/ECF system per Local Rule CV-5(b)(1) on July 8, 2013:

All others will be served via e-mail.

/s/ Alan D Albright

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JOINT CLAIM CONSTRUCTION CHART FOR DISPUTED CLAIM TERMS

U.S. Patent No. 5,467,455			
Claim Term	Claims	Plaintiff's Proposed Construction	Defendants' Proposed Construction
<i>dynamic termination circuitry</i>	22	“circuitry for signal termination that is selectively enabled or disabled in response to an enable signal whose assertion is based, at least in part, on the direction of data signals on the bus”	“signal termination circuitry that is allowed to be enabled only when data is incoming to the device”
<i>physically separated termination circuits</i>	22-24, 26	“distinct termination circuits”	Plain and ordinary meaning Alternatively, “one or more distinct termination circuits”
<i>terminal for communicating parallel binary data</i>	22, 26	“a plurality of external pins communicating parallel binary data”	Plain and ordinary meaning Alternatively, “a connection for communicating parallel binary data”
<i>“at least one device”</i> <i>or</i> <i>“one device”</i>	22,27	<i>“at least one device”</i> : No construction necessary (plain and ordinary meaning)	<i>“one device”</i> : “a single circuit element, such as a single transistor, within each termination circuit”

U.S. Patent No. 5,467,455			
Claim Term	Claims	Plaintiff's Proposed Construction	Defendants' Proposed Construction
<i>optimal impedance</i>	28	“the proper impedance, selected from among a plurality of possible impedances within a given system, for reducing signal reflections on a transmission line or bus”	“the best impedance, selected from among a plurality of possible impedances within a given system, for reducing signal reflections on a transmission line or bus”
<i>read/write signal that indicates when the integrated circuit is being subject to a read or write operation</i>	28	No construction necessary (plain and ordinary meaning)	“a signal that takes one logic value indicating a read operation and a different logic value indicating a write operation”
<i>determining an optimal impedance required for the plurality of terminals</i>	28	“selecting an optimal impedance among a group of possible impedances required for the plurality of terminals”	This claim is invalid for lacking a sufficient supporting written description and for a lack of enabling disclosure under 35 U.S.C. §112, ¶1.

JOINT CLAIM CONSTRUCTION CHART FOR DISPUTED CLAIM TERMS

U.S. Patent No. 5,943,274			
Claim Term	Claims	Plaintiff's Proposed Construction	Defendants' Proposed Construction
<i>level converter</i>	1, 6, 9	"a circuit that converts inputs at one level to outputs at a different level"	"a circuit that converts small signal inputs from the differential amplifier to nearly CMOS level outputs to the clock-free latch"
<i>impedance control circuit</i>	1, 11	"a circuit that selectively provides a high impedance state"	"a circuit that provides a high impedance state at the output of the level converter"
<i>switching element</i>	11	"a circuit element performing a switching function"	Plain and ordinary meaning Alternatively, "a circuit element that has a conducting state and a non-conducting state"
<i>level converting</i>	14, 20	"converting inputs at one level to outputs at a different level"	"converting small signal inputs from the amplifying step to nearly CMOS level outputs to the clock-free latch"
<i>change in impedance</i>	14, 20	No construction necessary (plain and ordinary meaning)	"a transition between a high impedance state and a low impedance state"

JOINT CLAIM CONSTRUCTION CHART FOR DISPUTED CLAIM TERMS

U.S. Patent No. 6,920,316			
Claim Term	Claims	Plaintiff's Proposed Construction	Defendants' Proposed Construction
<i>protection device</i>	6,7	"an electrostatic discharge protector"	This claim term should not be construed separately from the clause "a protection device for protecting said input capacitor from damage during an electrostatic discharge event," which is a means-plus-function clause under 35 U.S.C. 112 ¶6. See below.
<i>a protection device for protecting said input capacitor from damage during an electrostatic discharge event</i>	6,7	<p>The phrase is not a means-plus-function clause under 35 U.S.C. § 112, ¶6. "Protection device" is defined above; no further construction is necessary (plain and ordinary meaning).</p> <p>To the extent the Court determines that the phrase is a means-plus-function clause, then in the alternative:</p> <p><u>Structure</u>: electrostatic discharge protector</p> <p><u>Function</u>: protecting the input capacitor from damage during an electrostatic discharge event</p>	This clause is a means-plus-function clause under 35 U.S.C. §112, ¶6. There is no corresponding structure in the specification, so the claim is indefinite.

JOINT CLAIM CONSTRUCTION CHART FOR DISPUTED CLAIM TERMS

U.S. Patent No. 7,927,927			
Claim Term	Claims	Plaintiff's Proposed Construction	Defendants' Proposed Construction
<i>arranged in an array</i>	1, 11	No construction necessary (plain and ordinary meaning) Alternatively, "positioned in a row and column format"	"positioned in a row and column format and including all package sites located in each row and column"
<i>a singulation space</i>	1, 11	No construction necessary (plain and ordinary meaning) Alternatively, "a separation space"	"all portions of the substrate separating the individual package sites in the array"
<i>a rigid printed circuit board substrate</i>	1, 11	"a printed circuit board substrate that is reinforced with fibers"	Indefinite; see Defendants' Amended Invalidity Contentions for the '927 Patent
<i>forming a cavity containing the plurality of substantially identical package sites</i>	1, 11	No construction necessary (plain and ordinary meaning) Alternatively, "placing or forming a barrier on the substrate that surrounds the plurality of substantially identical package sites to define a space"	"placing or forming a barrier on the substrate that surrounds the array of substantially identical package sites to define a space with an open top for holding the encapsulant"
<i>overmolding</i>	1, 2, 11, 12	"forming encapsulating material in a cavity of a defined shape over one or more components on only one side of a substrate"	"placing a mold on the barrier to close the open top of the space whereby the mold defines the top surface of the encapsulant in the space"

U.S. Patent No. 7,927,927			
Claim Term	Claims	Plaintiff's Proposed Construction	Defendants' Proposed Construction
<i>[overmolding] a single and continuous encapsulant over each semiconductor device, the plurality of sites, and the singulation space</i>	1	"overmolding" is defined above; no further construction is necessary (plain and ordinary meaning). Alternatively, a construction for "a singulation space" is provided above	"covering each and every semiconductor device, each and every site in the array, and the singulation space with a layer of encapsulant"
<i>[overmolding] an encapsulant over the plurality of sites and the singulation space</i>	11	"overmolding" is defined above; no further construction is necessary (plain and ordinary meaning). Alternatively, a construction for "a singulation space" is provided above	"covering each and every semiconductor device, each and every site in the array, and the singulation space with a layer of encapsulant"
<i>a top surface</i>	1, 11	"the outermost surface of the encapsulant on a packaged semiconductor device"	Ordinary meaning / no construction required
<i>a top surface planarity deviation</i>	11	"the difference between the average height of the entire top surface and the point most removed from the average"	See below; term should be construed in context
<i>surface deviation</i>	1		
<i>[a top surface of the continuous encapsulant which has] a surface deviation of less than 0.13 millimeters across the top surface of the continuous encapsulant</i>	1	"surface deviation," "top surface," and "a top surface planarity deviation" are defined above; no further construction is necessary (plain and ordinary meaning)	Indefinite; see Defendants' Amended Invalidity Contentions for the '927 Patent Alternatively,
<i>a top surface planarity deviation of less than 0.13 millimeters</i>	11		"the difference between the highest point and lowest point of the top surface of the encapsulant is less than 0.13 millimeters"